Agilent M9703A

AXIe High-Speed Digitizer/
Wideband Digital Receiver

Data Sheet

8 channels, 12-bit, up to 3.2 GS/s,
DC up to 2 GHz input frequency range

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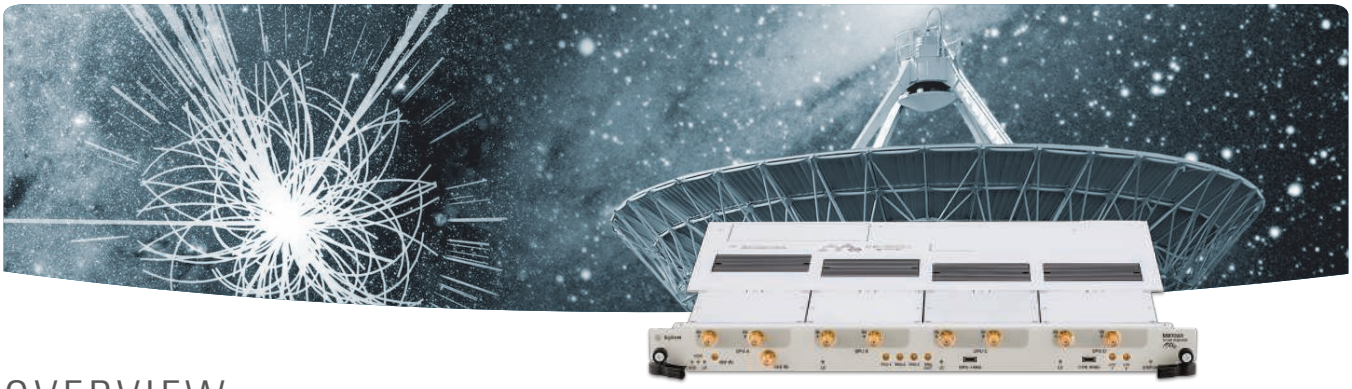

OVERVIEW

Introduction

The Agilent M9703A is a very fast versatile DC-coupled 12-bit wideband digital receiver/digitizer, providing exceptional measurement fidelity over multiple phase coherent channels. Based on the AXIe standard, offering eight acquisition channels in a single-slot card, it provides excellent channel density and flexible scalability. These features allow the implementation of a large number of high dynamic range, phase-coherent channels in a small volume, making the M9703A high-speed digitizer/wideband digital receiver ideal for multi-channel applications in advanced physics, aerospace & defense, and RF communications.

Product description

The Agilent M9703A is a revolutionary 8-channel, 12-bit wideband digital receiver/digitizer, implementing a patented front-end able to capture signals from DC up to 2 GHz at 1.6 GS/s, with exceptional measurement accuracy. An interleaving capability allows two channels to be combined to acquire at 3.2 GS/s on four channels with more than 1 GHz instantaneous bandwidth.

The M9703A wideband digital receiver/digitizer also provides very long on-board acquisition memory and real-time data processing capability with four Virtex 6 FPGAs.

The on-board FPGAs can feature an optional real-time digital downconverter (DDC) that allows tuning and zooming on the signal to be analyzed. The DDC functionality improves the dynamic range, reduces the noise floor, extends the capture time, and accelerates the measurement speed.

The M9703A high-speed digitizer can also be combined with the Agilent 89600 VSA software for advanced multi-channel signal analysis.

Example applications

- Advanced research experiments such as hydrodynamics or plasma fusion
- Radar and satellite communication applications such as antenna array calibration/test, passive radar receiver, or multi-band SATCOM monitoring
- Emerging standards (5G) R&D and DVT in massive MIMO, or multichannel BaseBand IQ

Product features

- 8 channels (4 when interleaving) with 12-bit resolution
- Up to 3.2 GS/s sampling rate (with -SR2 and -INT options)
- DC to 2 GHz input frequency range (with -F10 option in non interleaved acquisition)
- Accurate time-to-trigger interpolator (TTI)
- Up to 16 GB (1 GSamples/ch) on-board memory
- PCIe backplane providing 1.1 GB/s data transfer speed
- 4 configurable Virtex-6 FPGAs
- Real-time digital downconversion (DDC)
  - 8 phase-coherent channels with independent local oscillators (LO) setting, tunable with 0.01 Hz resolution
  - Adjustable analysis bandwidth from 300 MHz down to less than 1 kHz
  - Magnitude trigger

Uncompromising values

- Very wide bandwidth and fast acquisition with optimized dynamic range
- Get toward a fully digital receiver
- Scalable phase-coherent acquisition channels in a small space
- High measurement throughput
- Open FPGA for custom processing
- Reduced test time by tuning and zooming on signals (requires -DDC option)
  - Isolate the signal of interest
  - Improve the dynamic range
  - Extend the capture time, or reduce the amount of transferred data
  - Trigger on the signal of interest

Hardware platform

Product overview

The M9703A is a flexible modular wideband digital receiver/digitizer offering scalable features depending on application requirements. The standard configuration implements 8 channels of 12-bit resolution with DC to 650 MHz input frequency range (–3 dB analog bandwidth), and acquiring data at 1 GS/s. If higher speed is required, the -SR2 option enables the eight channels to sample at 1.6 GS/s. An interleave option (-INT) also allows two channels to be combined and reach 3.2 GS/s in 4-channel acquisition mode. For higher frequency signals, the -F10 option provides an extended input frequency range of DC up to 2 GHz in non interleaved mode, or DC to > 1 GHz when interleaving channels [1].

For applications where the dynamic range and signal sensitivity is critical, the -FRF option provides optimized analog performance for the best measurement integrity.

Data processing

The M9703A implements Xilinx Virtex-6 FPGAs dedicated to data processing. The four data processing units (DPU) implement a standard digitizer functionality firmware by default, allowing digitization of the signal, storage of the resulting data in the on-board memory and transfer through the PCIe backplane bus.

The four DPUs may optionally feature a real-time digital down-conversion (DDC) IP algorithm if ordered with the -DDC or the -LDC options. The DDC allows tuning and zooming on the signals to be analyzed, improving the dynamic range, reducing the noise floor, extending the capture time, and accelerating the measurement speed.

The -LDC option is especially suited for MIMO and multi-channel BBIQ applications. It provides up to 80 MHz of real-time frequency span (analysis bandwidth) per channel when combined with the -SR2 option (up to 50 MHz with -SR1).

For demanding applications, the -DDC option extends the real-time frequency span/analysis bandwidth to up to 300 MHz. Both -LDC and -DDC allow to vary the center frequency from DC to 1.6 GHz [2] independently per channel.

The M9703A also provides open access to its on-board processing FPGAs for custom algorithm implementation. This can be reached through the SystemVue software W1462BP FPGA Architect, providing an automatic push button programming approach.

Block diagram

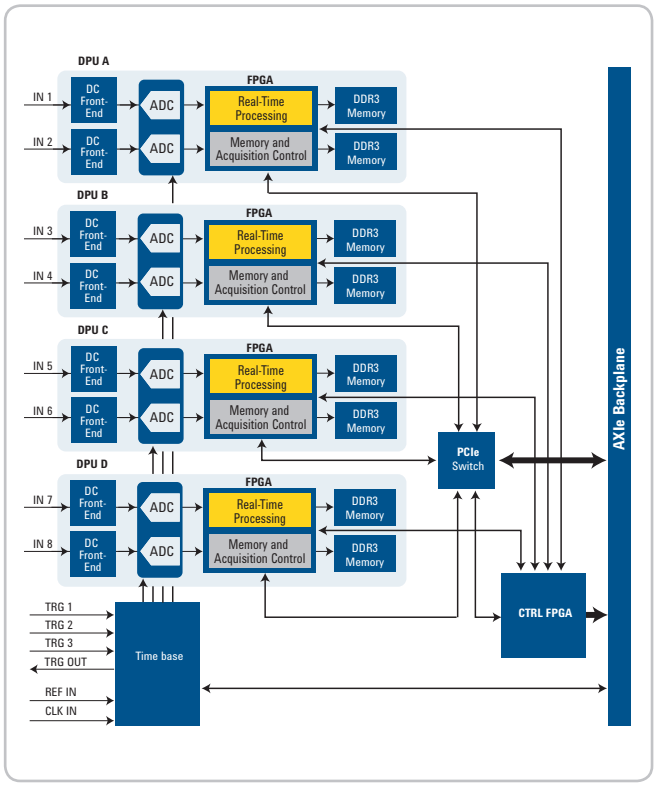

Figure 1. Simplified block diagram of the M9703A AXIe Digitizer.

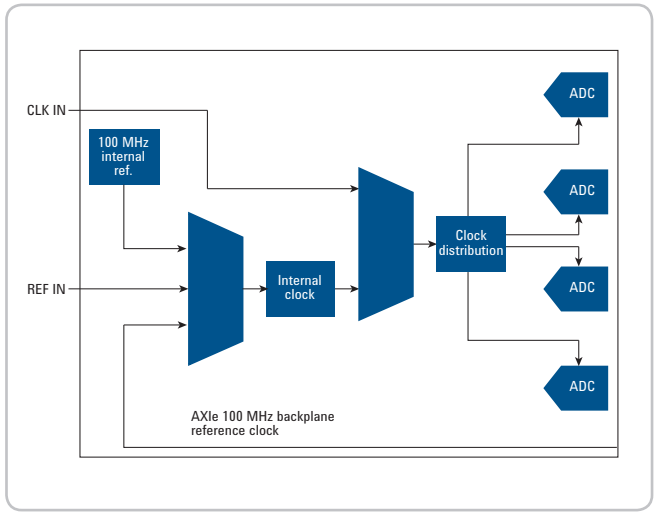

Figure 2. M9703A clocking mode simplified block diagram.

[1] *The fact that there is less frequency range when interleaving channels is due to internal characteristics of the analog-to-digital converter chipset that filters at 1 GHz when combining channels.*

[2] *If -F10 option is ordered, otherwise limits to 650 MHz.*

Software platform

IO libraries

Agilent IO Libraries Suite offers FAST and EASY connection to instruments using a standardize interface and ensure compatibility as well as upgradability of the software applications.

The Agilent IO Libraries Suite helps you by displaying ALL of the modules in your system. From here you can view information about the installed software or launch the modules' soft front panel directly from Agilent Connection Expert (ACE).

In addition, ACE offers an easy way to find the correct driver for your instrument.

Drivers

The M9703A AXIe digitizer is supplied with a comprehensive portfolio of module drivers, documentation, examples, and software tools to help you quickly develop test systems with your software platform of choice. The module comes with IVI-C, IVI-COM, and LabVIEW software drivers to work in the most popular development environments, such as MATLAB, LabVIEW, Microsoft C/C++ or C#. These drivers are provided for Windows and Linux operating systems.

Easy software integration

To help you get started and complete complex tasks quickly, the module software is provided with context sensitive help, complete documentation and code examples that allow a quick module set up and basic acquisition functionalities. These code examples can be easily modified, so that the card can be quickly integrated into a measurement system. Included are application code examples for LabVIEW, LabWindows/CVI, Visual Studio C, C++, and C#, and MATLAB which provide digitizer set up and basic acquisition functionality.

Compliance

The M9703A is compliant with AXIe and AdvancedTCA (ATCA) formats. Designed to benefit from fast data interfaces, the product can be integrated into AXIe or ATCA chassis slots. Based on ATCA, the AXIe standard implements extensions for instrumentation and test, and uses clever techniques to add powerful timing features.

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Software applications

In addition, the M9703A includes the Agilent MD1 soft front panel (SFP) graphical interface. This simple software application can be used to control, verify the functionality and explore the capabilities of the Agilent modular high-speed digitizers.

For advanced measurement analysis, the M9703A AXIe wideband digital receiver/digitizer can be combined with Agilent's 89600 Vector Signal Analysis software, the industry's standard for signal analysis and demodulation.

Thanks to the exceptional data throughput (1.1 GB/s) of its PCIe backplane bus, the M9703A allows a much faster connection to the 89600 VSA software, compared to traditional instruments.

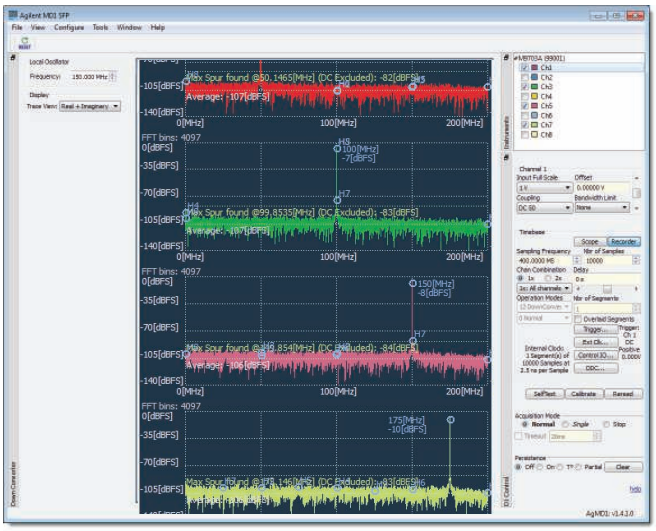


Figure 3. Agilent M9703A MD1 software front panel (SFP) interface.

The M9703A digitizer is also supported by Agilent SystemVue electronic design automation (EDA) environment software. The SystemVue EDA software includes rich processing libraries, enabling system architects and algorithm developers in wireless and aerospace/defense communications to innovate. When coupling the M9703A wideband digital receiver with SystemVue W1462 FPGA Architect, designers have at their disposal an open FPGA development environment for custom on-board processing. This solution allows a complete, integrated design-to-test flow, dramatically cutting design to prototyping time and verification effort.

Front-end options

The M9703A wideband digital receiver/digitizer provides a range of front-end options to adapt the digitization to the particular application requirements. These options are divided in three categories:

- **Bandwidth**

  The instantaneous analog bandwidth is the –3 dB compression point of the analog front-end frequency response. The M9703A provides two levels of instantaneous analog bandwidth. The default -F05 option provides an input frequency range of DC to 650 MHz, especially suited for baseband applications (e.g. BBIQ). If more bandwidth is required, or for higher IF frequency signals, the -F10 option provides an extended input frequency range up to 2 GHz (in non-interleaved mode)[1].

- **Sampling rate**

  The standard configuration of the product includes the -SR1 option, allowing digitization at 1 GS/s. The -SR2 option increases this rate to 1.6 GS/s, and if even higher sampling rates are required, the -INT option allows interleaving of the input channels providing 3.2 GS/s on four acquisition channels.

- **Front-end analog performance**

  The M9703A wideband digital receiver/digitizer provides exceptional analog-to-digital conversion performance in its standard configuration, with very high dynamic range and low noise. In some applications, every dB of dynamic range is critical, and for those applications, the -FRF option pushes the analog performance optimization further in order to reach even better dynamic range, and signal sensitivity.

Figure 4. Noise power spectral density (NSD) measured with the 89600 VSA software on one channel of the M9703A. With a very low NSD down to –145 dBm/Hz, the M9703A has comparable performance to some 16-bit digitizers.

[1] *DC to 1.4 GHz when interleaving channels.*

Firmware options

The M9703A high-speed digitizer provides various firmware options:

- **-DGT**: Digitizer firmware (standard)
- **-DDC**: Wideband real-time digital downconversion
- **-LDC**: Limited-bandwidth real-time digital downconversion
- **-FDK**: On-board FPGA programming access

The -DGT option features a standard digitizer firmware that is included in the default configuration. The digitizer firmware allows standard data acquisition, including: digitizer initialization, setting of the acquisition and clocking modes, management of channel synchronization, storing the data in the internal memory and/or transferring them through the backplane bus. The digitizer firmware also implements segmented acquisition functionality.

The real-time digital downconversion (DDC) options -LDC and -DDC, in addition to the basic digitizer functionality, implement a real-time digital decimation and filtering on the digitized data, allowing the user to tune and zoom on the signals of interest. This exclusive IP algorithm provides very powerful and flexible digital downconversion on all 8 channels. The filters and local oscillators (LO) are synchronized to maintain constant phase and timing relationships allowing phase-coherent post processing. The DDC provides three main functions:

- **Data reduction (zoom)**

  Reducing the bandwidth and sample rate to match the analyzed signal decreases the amount of data that needs to be transferred for a given capture duration, in turn accelerating post-processing operations.

- **Frequency shifting (tune)**

  Independently shifting each channels IF signal into baseband, allows the analysis bandwidth to be set around the signal of interest.

- **Magnitude trigger**

  Setting the magnitude level that a signal needs to achieve at a specified frequency and bandwidth allows triggering only on the signal of interest.

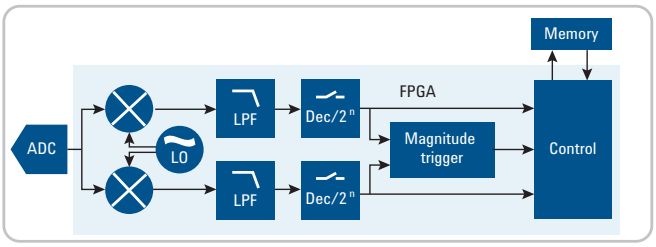


Figure 5. Single channel digital downconverter (DDC) simplified block diagram.

Firmware options, continued

These three functions allow isolation of the signal of interest from other signals in a crowded spectrum, improved dynamic range as the integrated noise is reduced, and increased SNR and effective number of bits (ENOB). The resulting advantage for your application is a reduced test time, while improving overall test efficiency.

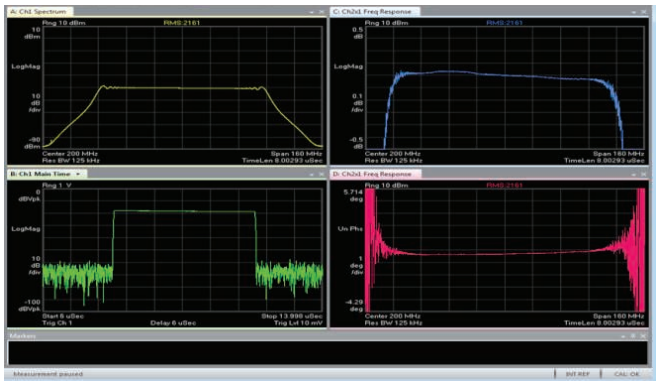


Figure 6. The excellent channel-channel phase coherency, coupled with the wideband and flexible capability of the -DDC option, allows exceptionally fast and accurate cross-channel measurements on a large variety of signals, such as multi-tone, wideband frequency chirps, or complex signals. In this case, we show the measurement of cross-channel phase and amplitude for a 160 MHz frequency chirp.

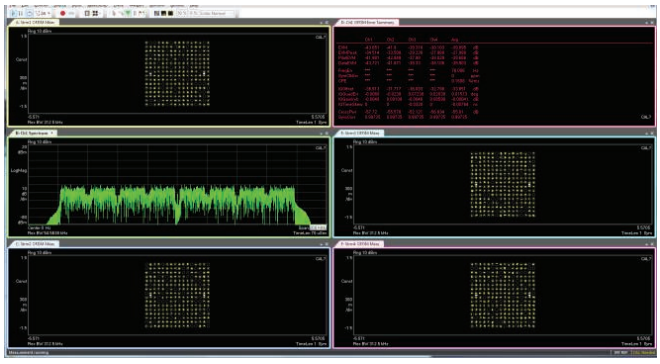
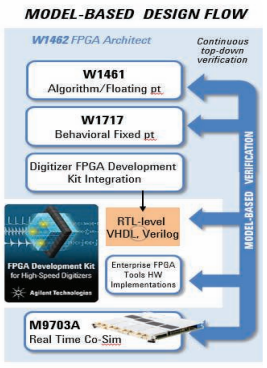


Figure 7. The M9703A-LDC option provides real-time digital downconversion for up to 80 MHz frequency span per channel (160 MHz in I+jQ mode), ideal for emerging communications standards research and design validation.Here we show the analysis of four 802.11ac 160 MHz wide baseband signals. The M9703A allows to reach an EVM of down to –45 dB.

The wideband capability of the M9703A, combined with its excellent signal sensitivity and dynamic range is a step toward a fully digital receiver, by reducing or suppressing the analog mixer stages. As an example, the M9703A wideband digital receiver/digitizer can directly digitize DVB-T signals, especially interesting for passive radar applications. When combined with the M9362A-D01 quad-channel downconverter, the M9703A allows capture and analysis of wideband signals up to 50 GHz.

Figure 8. The M9703A wideband digital receiver allows to directly digitize DVB-T signals with excellent dynamic range without the need of analog mixers, especially interesting for passive radar applications.

The -FDK option allows the access to the four on-board processing FPGAs for custom algorithm implementation. The FPGA programming is reached via the W1462 SystemVue FPGA Architect, and excludes the usage of other M9703A firmware options (such as the DDC).



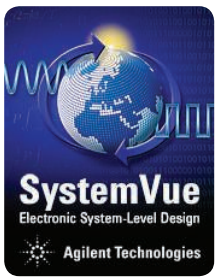


Figure 9. SystemVue software model-based design flow.

TECHNICAL SPECIFICATIONS AND CHARACTERISTICS

Analog input (IN1 to IN8 SMA connectors)			
Number of channels			8 (eight), 8 or 4 (with INT option)
Impedance			50 Ω ±2 %
Coupling			DC
Full scale ranges (FSR)			1 V and 2 V (3.98 dBm and 10 dBm)
Maximum input voltage			1V FSR: 3 V RMS, ± 3.6 Vpk 2V FSR: 4.3 V RMS, ± 6.3 Vpk
Input frequency range (–3 dB bandwidth)			DC to 1.9 GHz *(typical)* in 1V FSR at 1 GS/s or 1.6 GS/s DC to 2.0 GHz *(typical)* in 2V FSR at 1 GS/s or 1.6 GS/s DC to 1.4 GHz *(typical)* at 2 GS/s or 3.2 GS/s
DC gain accuracy			± 0.5% *(typical)*
Offset accuracy			± 0.5% in 1V FSR ± 1.5% in 2V FSR
Time skew [1]	Channel-to-channel skew [2]		± 50 ps *(nominal)* in same module ± 150 ps *(nominal)* between multiple modules of same chassis
	Channel-to-channel skew stability [3]		± 200 fs pk *(nominal)* 75 fs RMS *(nominal)*
Phase offset	Channel-to-channel offset (@ 400 MHz)		± 7.2° *(nominal)* in same module ± 21.6° *(nominal)* between multiple modules of same chassis
	Channel-to-channel offset stability [3]		± 0.03° pk *(nominal)* 0.01° RMS *(nominal)*
Input voltage offset			–2xFSR to +2xFSR
Bandwidth limit filters (BWL)			650 MHz *(nominal)*
Frequency response flatness			± 1 dB from DC to 650 MHz
Standard front-end configuration			
Effective bits (ENOB) [4]		@ 48 MHz	9.0 *(typical)*
		@ 100 MHz	9.1 *(typical)*
		@ 410 MHz	8.2 *(8.9, typical)*
Signal to Noise Distortion (SNR) [4]		@ 48 MHz	58 dB *(typical)*
		@ 100 MHz	58 dB *(typical)*
		@ 410 MHz	54 dB *(56 dB, typical)*
Spurious Free Dynamic Range (SFDR) [4]		@ 48 MHz	59 dBc *(typical)*
		@ 100 MHz	63 dBc *(typical)*
		@ 410 MHz	52 dBc *(60 dBc, typical)*
Total Harmonic Distortion (THD) [4]		@ 48 MHz	–59 dB *(typical)*
		@ 100 MHz	–62 dB *(typical)*
		@ 410 MHz	–60 dB *(typical)*
Noise spectral density (NSD)			–146 dBm/Hz *(nominal)*

[1] The channel-to-channel skew is defined as the magnitude of time delay difference between two digitized channel inputs, granted the same signal is provided to each channel at the exact same time.

[2] The measurement represents the maximum time skew, measured with a Sinefit method on 100k samples, for a sinusoid signal at 400 MHz and averaged 10 times.

[3] Skew and offset stability are measured at 25 °C in a climatic chamber. The skew and offset between channels are measured every 5 minutes over 12 hours and after 1hour stabilization time and the values represent the dispersion of the measurements. Valid for channels within a same module and accross modules of a same chassis.

[4] Measured at 1.6 GS/s for a -1 dBFS input signal in internal clock mode with F10 option.

Analog input (IN1 to IN8 SMA connectors), continued

With -FRF option (optimized dynamic range)

Effective bits (ENOB) [1]	@ 48 MHz	8.7 *(9.1, typical)*
	@ 100 MHz	8.8 *(9.2, typical)*
	@ 410 MHz	8.8 *(9.1, typical)*
	@ 650 MHz	8.7 *(9.0, typical)*
	@ 925 MHz	8.3 *(8.8, typical)*
Signal to Noise Distortion (SNR) [1]	@ 48 MHz	56 dB *(58 dB, typical)*
	@ 100 MHz	56 dB *(58 dB, typical)*
	@ 410 MHz	55 dB *(58 dB, typical)*
	@ 650 MHz	54 dB *(57 dB, typical)*
	@ 925 MHz	52 dB *(55 dB, typical)*
Spurious Free Dynamic Range (SFDR) [1]	@ 48 MHz	55 dBc *(60 dBc, typical)*
	@ 100 MHz	60 dBc *(65 dBc, typical)*
	@ 410 MHz	58 dBc *(63 dBc, typical)*
	@ 650 MHz	58 dBc *(64 dBc, typical)*
	@ 925 MHz	56 dBc *(61 dBc, typical)*
Total Harmonic Distortion (THD) [1]	@ 48 MHz	–60 dB (*typical*)
	@ 100 MHz	–62 dB (*typical*)
	@ 410 MHz	–62 dB (*typical*)
	@ 650 MHz	–64 dB (*typical*)
	@ 925 MHz	–61 dB (*typical*)

Baseband IQ (BBIQ) characteristics

Nominal EVM using Agilent 89600B VSA software		
SISO 802.11ac 256QAM	80 MHz BW	–45 dB (*nominal*) without correction filter –47 dB (*nominal*) with correction filter
	160 MHz BW	–43 dB (*nominal*) without correction filter –45 dB (*nominal*) with correction filter
MIMO 802.11ac 256QAM, 2x2	80 MHz BW	–45 dB (*nominal*) without correction filter
	160 MHz BW	–43 dB (*nominal*) without correction filter
MIMO 802.11ac 256QAM, 4x4	80 MHz BW	–44 dB (*nominal*) without correction filter
	160 MHz BW	–42 dB (*nominal*) without correction filter
SISO LTE-A FDD DL, 2CCs full filled 64QAM	2x20 MHz BW	–50 dB (*nominal*) without correction filter
SISO LTE-A FDD DL, 4CCs Full filled 64QAM	4x20 MHz BW	–47 dB (*nominal*) without correction filter
SISO LTE-A FDD DL, 5CCs Full filled 64QAM	5x20 MHz BW	–45 dB (*nominal*) without correction filter
SISO 64 point FFT OFDM	800 MHz BW	–42 dB (*nominal*) with correction filter

RF characteristics

Nominal EVM using Agilent 89600B VSA software		
GSM BTS signal	@ 900 MHz @ 1.8 GHz	–51 dB (*nominal*) –48 dB (*nominal*)
DVB-T signal	10 MHz BW @ 850 MHz	–53 dB (*nominal*)
Spurious-free dynamic range (SFDR) nominal performance measured with Agilent 89600B VSA software [2]		
SFDR	30 MHz BW @ 900 MHz	–92 dBc (*nominal*)
	80 MHz BW @ 900 MHz	–90 dBc (*nominal*)
	100 MHz BW @ 400 MHz	–92 dBc (*nominal*)
	400 MHz BW @ 400 MHz	–87 dBc (*nominal*)
	625 MHz BW @ 400 MHz	–83 dBc (*nominal*)

[1] *Measured at 1.6 GS/s for a –1 dBFS input signal in internal clock mode with F10 option.*

[2] *Measured for a CW signal of –10 dBm at the center frequency of the analyzed frequency span (BW).*

TECHNICAL SPECIFICATIONS AND CHARACTERISTICS, CONTINUED

Digital conversion

Resolution			12 bits
Acquisition memory (total)		Standard -M40 -M16	1 GB (64M real samples/ch) 4 GB option (256M real samples/ch) 16 GB option (1G real samples/ch)
Sample clock sources			Internal or external
Internal clock source			Internal, external or backplane reference
	Max. real-time sampling rates	Standard -SR2 -INT -INT, -SR2	1 GS/s per channel 1.6 GS/s per channel option 1-2 GS/s option 1.6-3.2 GS/s option
	Sampling jitter		225 fs *(nominal)* [1]
	Clock accuracy		±1.5 ppm
External clock source (CLK IN SMA connector)			
	Impedance		50 Ω *(nominal)*
	Frequency range [2]	Standard -SR2	1.8 GHz to 2 GHz 1.8 GHz to 3.2 GHz
	Signal level		+5 dBm to +15 dBm *(nominal)*
	Coupling		AC
External reference clock (REF IN MCX connector)			
	Impedance		50 Ω *(nominal)*
	Frequency range		100 MHz ±5 kHz *(nominal)*
	Signal level		–3 dBm to +3 dBm *(nominal)*
	Coupling		AC
Acquisition modes			Single shot, sequence (up to 65536 segments. Segment maximum length = memory size/number of channels)

Trigger

Trigger modes			Edge (positive, negative), level, magnitude [3]
Trigger sources			External, Software, channel
Channel trigger frequency range			DC to 250 MHz
External trigger (TRG 1, TRG 2, TRG 3 MCX connectors)			
	Coupling		DC
	Impedance		50 Ω *(nominal)*
	Level range		± 5 V *(nominal)*
	Amplitude		0.5 V pk-pk
	Frequency range		DC to 2 GHz
Maximum time stamp duration	-SR1 -SR2		52 days 32 days
Trigger time interpolator resolution	-SR1 -SR2		7.75 ps *(nominal)* 6.25 ps *(nominal)*
Trigger time interpolator precision	-SR1 -SR2		20.7 ps RMS *(nominal)* 15 ps RMS *(nominal)*
Rearm time	Digitizer mode DDC mode		0.8 us *(nominal)* 2.5 us
Trigger out (TRG OUT MCX connector) [4]			
Signal level			1.15 Vpk–pk *(nominal)*
Rise/fall time			9 ns / 19 ns *(nominal)*

[1] Jitter figure based on phase noise integration from 100 Hz to 1600 MHz.

[2] The sampling rate corresponds to half of the external clock frequency in 8-channel mode (non interleaved channels). In interleaved mode (only available with the INT option), the sampling rate corresponds to the frequency of the external clock signal.

[3] Only with -DDC option.

[4] At 10 MHz on a 50 Ω load.

TECHNICAL SPECIFICATIONS AND CHARACTERISTICS, CONTINUED

Real-time digital downconversion (-LDC and -DDC options)

Acquisition modes	Basic digitizer or DDC digitizer [1, 2]
Number of synchronous DDC channels	8 in a single module Up to 40 across 5 modules in a same M9505A chassis
Frequency tuning range (LO)	DC to 1.6 GHz (with -F10)
Center frequency tuning resolution	0.01 Hz
Independent channel center frequency tuning	Yes
Independent channel frequency span	No

	Decimated sampling rate				Analysis bandwidth				Maximum acquisition memory time			
	-SR1		-SR2		-SR1		-SR2		-SR1		-SR2	
n	-LDC	-DDC	-LDC	-DDC	-LDC	-DDC	-LDC	-DDC	-LDC	-DDC	-LDC	-DDC
0	-	250 MS/s[3]	-	400 MS/s[3]	-	180 MHz[3]	-	300 MHz[3]	-	2.048 s	-	1.28 s
1	-	125 MS/s	-	200 MS/s	-	100 MHz	-	160 MHz	-	2.048 s	-	1.28 s
2	62.5 MS/s		100 MS/s		50 MHz		80 MHz		4.096 s		2.56 s	
3	31.25 MS/s		50 MS/s		25 MHz		40 MHz		8.192 s		5.12 s	
4	15.625 MS/s		25 MS/s		12.5 MHz		20 MHz		16.384 s		10.24 s	
5	7.812 MS/s		12.5 MS/s		6.25 MHz		10 MHz		32.768 s		20.48 s	
...	$(62.5/2^{n-2})$ MS/s		$(100/2^{n-2})$ MS/s		$(200/2^{n-2})$ MHz		$(320/2^{n-2})$ MHz		$(2.048*2^{n-2})$ s		$(1.28*2^{n-2})$ s	
18	0.238 kS/s		0.381 kS/s		0.763 kHz		1.22 kHz		536,871 s		335,544 s	

Control IO (I/O A and I/O B MMCX connectors)

Functions	Output	Acquisition active Trigger is armed Trigger accept resynchronization Low level High level

1. *The real-time DDC is active only for 1 GS/s and 1.6 GS/s sampling rate modes (non-interleaved mode).*
2. *In DDC mode, each sample is a pair or I & Q samples. Each sample is coded on 64 bits (32-bit I and 32-bit Q) when the decimation factor is >4, otherwise the coding is made on 32 bits (16-bit I and 16-bit Q).*
3. *Limited aliasing protection at 250 MS/s and 400 MS/s for signals wider than 250 MHz and 400 MHz respectively.*

TECHNICAL SPECIFICATIONS AND CHARACTERISTICS, CONTINUED

Environmental and physical [1]

Temperature Range	Operating Non-operating	0 °C to +45 °C –40 °C to +70 °C
EMC		Complies with European EMC Directive 2004/108/EC • IEC/EN 61326-1 • CISPR Pub 11 Group 1, class A • AS/NZS CISPR 11 • ICES/NMB-001 This ISM device complies with Canadian ICES-001. Cet appareil ISM est conforme a la norme NMB-001 du Canada.

Power dissipation

–48 V	Total Power
3.4 A *(typical)*	161 W *(typical)*, with -DGT option
3.6 A *(nominal)*	170 W *(nominal)*, with -DDC option

Mechanical characteristics

Form factor	1 slot AXIe
Size	30 mm W x 322.2 mm H x 280 mm D
Weight	3 kg (6.61 lbs)

System requirements

Operating systems	Windows XP, Service pack 3	Windows Vista, SP1 and SP2, Windows 7 (32-bit and 64-bit), All versions	Linux Kernel 2.6 or higher (32 or 64-bit), Debian 6.0, CentOS 5
Processor speed	600 MHz or higher required 800 MHz recommended	1 GHz 32-bit (x86), 1 GHz 64-bit (x64), no support for Itanium 64	As per the minimum requirements of the chosen distribution
Available Memory	256 MB minimum (1 GB or greater recommended)	1 GB minimum	As per the minimum requirements of the chosen distribution
Available Disk Space [3]	1.5 GB available hard disk space, includes: • 1 GB available for Microsoft .NET Framework 3.5 SP1 [2] • 100 MB for Agilent IO Libraries Suite	1.5 GB available hard disk space, includes: • 1 GB available for Microsoft .NET Framework 3.5 SP1 [2] • 100 MB for Agilent IO Libraries Suite	100 MB
Video	Super VGA (800x600) 256 colors or more	Support for DirectX 9 graphics with 128 MB graphics memory recommended (Super VGA graphics is supported)	Does not require graphics (headless system). X Windows with 1280x1024 recommended for SFP
Browser	Microsoft Internet Explorer 6.0 or greater	Microsoft Internet Explorer 7 or greater	Distribution supplied browser

[1] *Samples of this product have been type tested in accordance with the Agilent Environmental Test Manual and verified to be robust against the environmental stresses of Storage, Transportation and End-use; those stresses include but are not limited to temperature, humidity, shock, vibration, altitude and power line conditions. Test Methods are aligned with IEC 60068-2 and levels are similar to MIL-PRF-28800F Class 3.*

[2] *NET Framework Runtime Components are installed by default with Windows Vista. Therefore, you may not need this amount of available disk space.*

[3] *Because of the installation procedure, less disk space may be required for operation than is required for installation. The amount of spacelisted above is required for installation.*

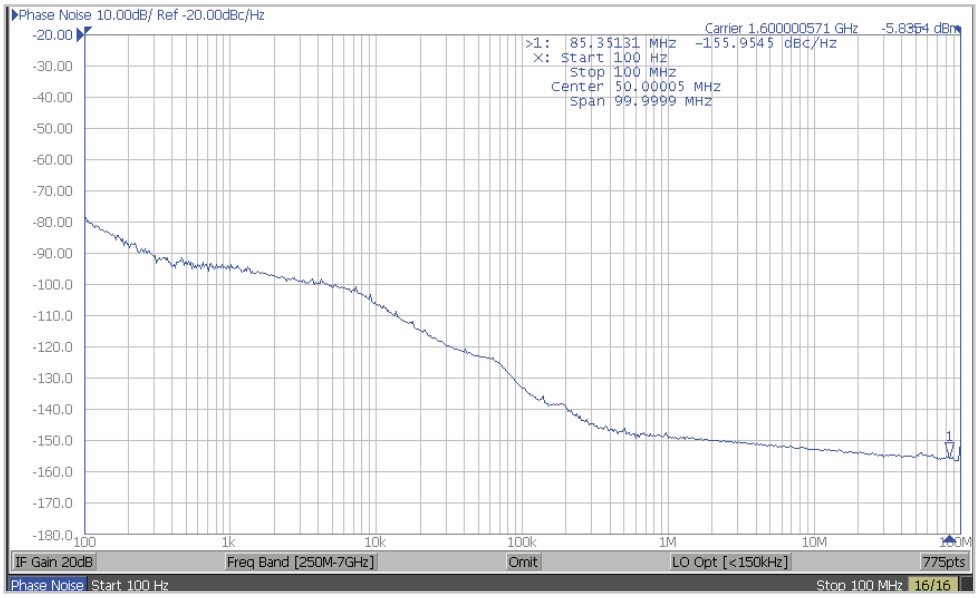


Figure 10. Measured sampling clock phase noise with an internal reference clock.

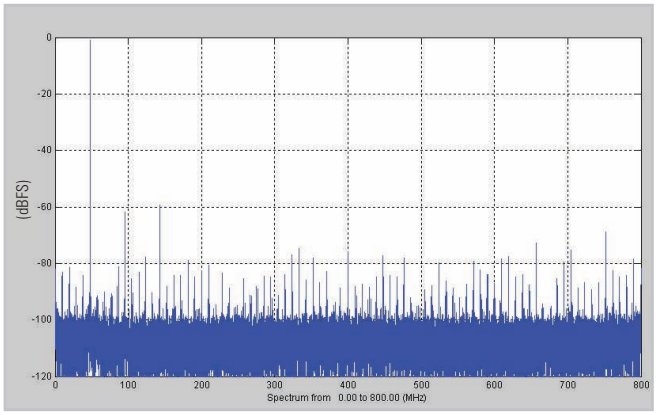


Figure 11. M9703A nominal dynamic performance in 1 V FSR for a –1 dBFS input signal at 48 MHz.

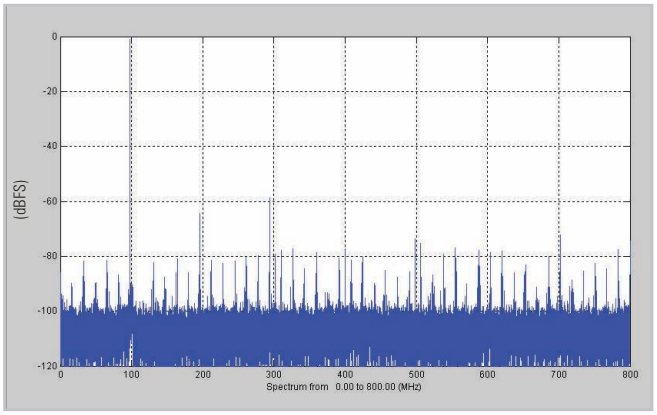


Figure 12. The FFT plot for a –1 dBFS input signal at 100 MHz in 1 V FSR shows the excellent dynamic range of the M9703A high-speed digitizer.

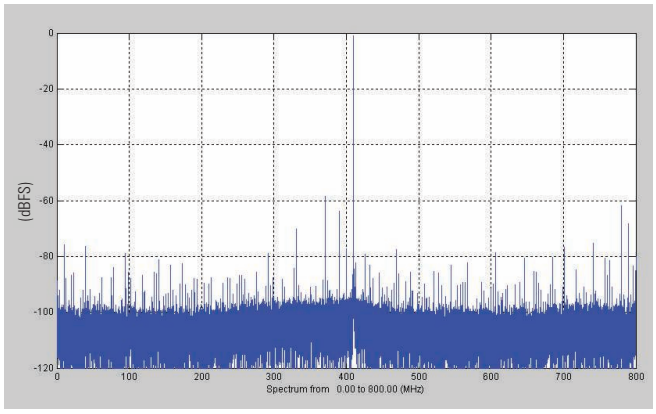


Figure 13. M9703A nominal dynamic performance in 1 V FSR for a –1 dBFS input signal at 410 MHz. Note how the dynamic range is still excellent for high frequency signals.

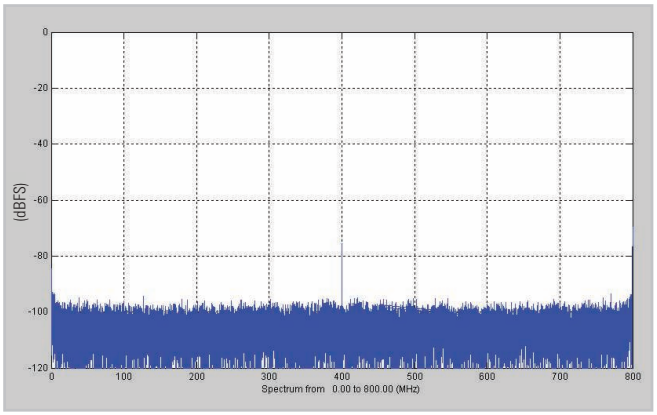


Figure 14. The M9703A nominal dynamic performance in 1 V FSR with no input signal (open input) shows a very low noise floor.

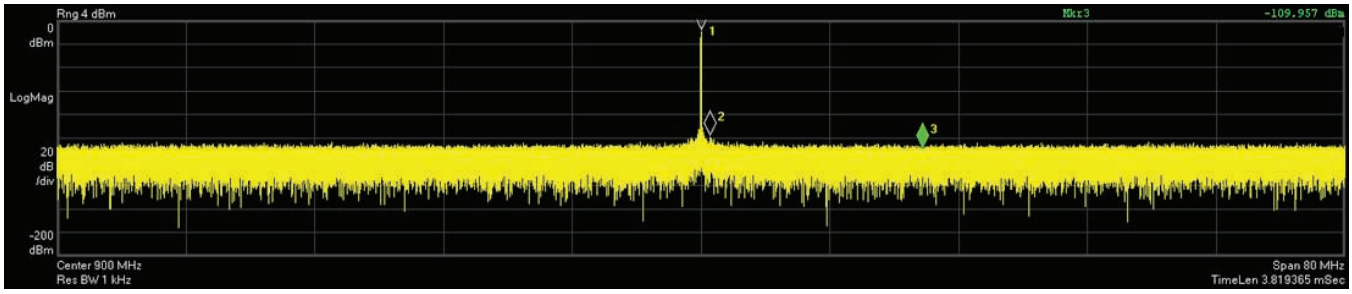


Figure 15. The exceptional noise power spectral density of the M9703A coupled with the real-time DDC allows the detection of very small signals. In this example, an 80 MHz span centered at 900 MHz, showing a very low noise floor of less than –100 dBm.

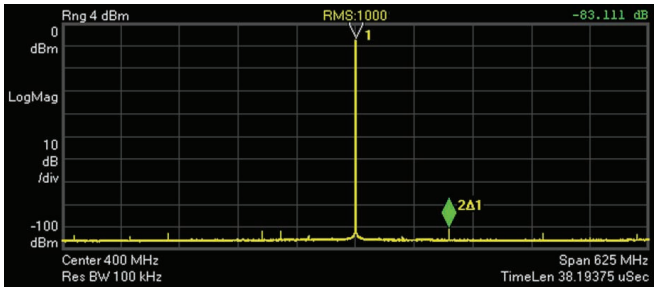


Figure 16. The M9703A has excellent dynamic range over a very wide bandwidth. In this example, the spectrum of a 400 MHz single tone signal, using the 89600 VSA software DDC, with 625 MHz frequency span centered at 400 MHz, showing -83 dBc SFDR.

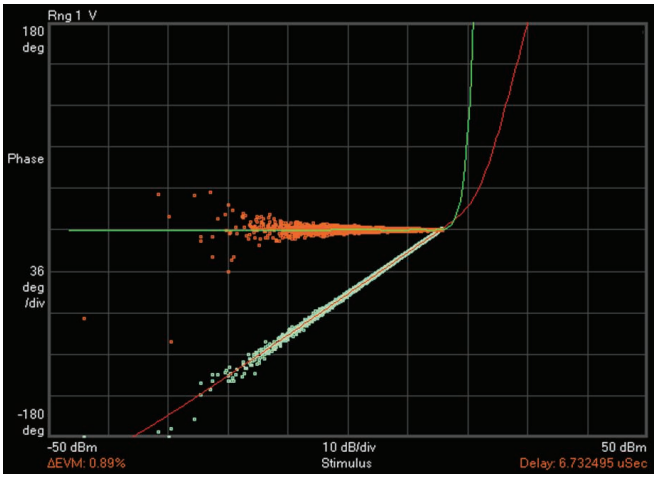


Figure 17. AM/AM and AM/PM characteristic for a 16QAM 250 MSym/s LTE signal at 400 MHz IF frequency and 400 MHz analyzed bandwidth.

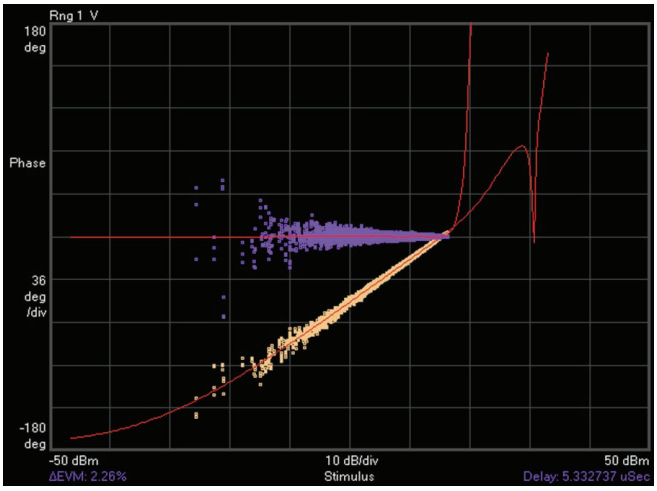


Figure 18. AM/AM and AM/PM characteristic for a 16QAM 500 MSym/s LTE signal at 400 MHz IF frequency and 625 MHz analyzed bandwidth.

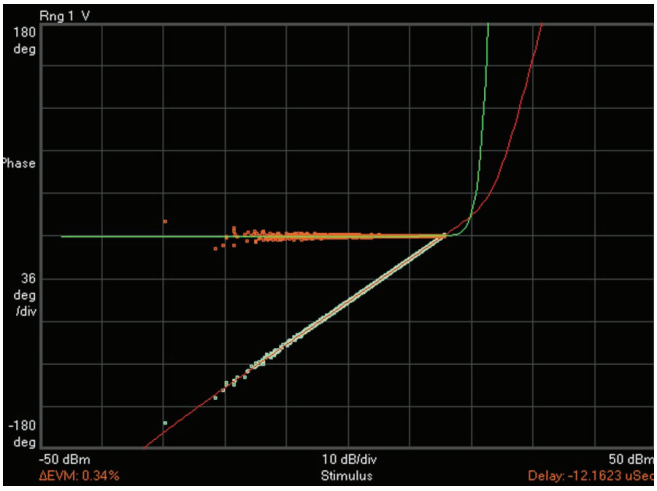
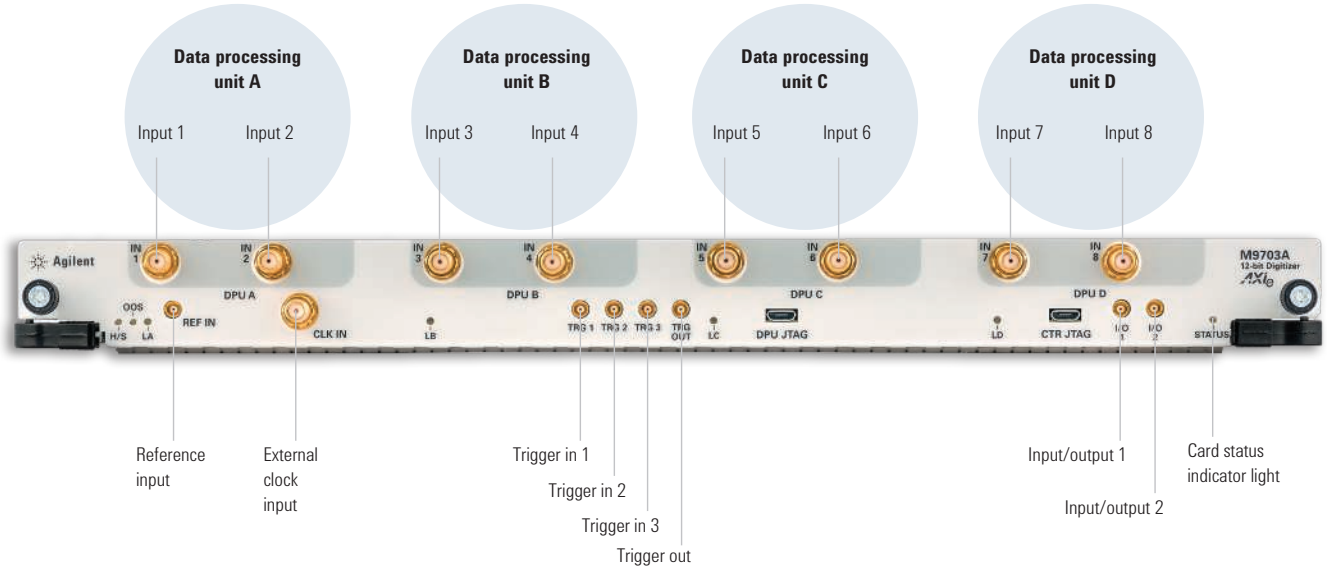


Figure 19. AM/AM and AM/PM characteristic for a 16QAM 20 MSym/s LTE signal with 400 MHz IF frequency and 100 MHz analyzed bandwidth.

Front panel connectors



Definitions for specifications

Specifications describe the warranted performance of calibrated instruments that have been stored for a minimum of 2 hours within the operating temperature range of 0 to 45 °C, unless otherwise stated, and after a 45 minute warm-up period. Data represented in this document are specifications unless otherwise noted.

Characteristics describe product performance that is useful in the application of the product, but that is not covered by the product warranty. Characteristics are often referred to as Typical or Nominal values.

- ***Typical*** describes characteristic performance, which 80% of instruments will meet when operated over a 20 to 30 °C temperature range. Typical performance is not warranted.

- ***Nominal*** describes representative performance that is useful in the application of the product when operated over a 20 to 30 °C temperature range. Nominal performance is not warranted.

Note: All graphs contain measured data from several units at room temperature unless otherwise noted.

Calibration intervals

The M9703A is factory calibrated and shipped with a calibration certificate.
Calibration is recommended every year in order to verify product performance.

CONFIGURATION AND ORDERING INFORMATION

Software information

Chassis slot compatibility: AXIe, ATCA	
Supported operating systems	Microsoft Windows XP (32-bit) Microsoft Windows 7 (32/64-bit) Microsoft Windows Vista (32/64-bit) Linux
Agilent IO libraries	Includes: VISA libraries, Agilent Connection Expert, IO Monitor

Related products

Model	Description
M9502A	2-slot AXIe chassis
M9505A	5-slot AXIe chassis
M9514A	14-slot AXIe chassis
M9536A	Embedded AXIe controller
U1092A	AcqirisMAQS Multichannel Acquisition Software
89601B	89600 VSA software, transportable license
W1462BP	SystemVue FPGA Architect

Figure 20. Five Agilent M9703A AXIe 12-bit digitizers installed in the Agilent M9505A 5-slot AXIe chassis to form a 40-channel 12-bit acquisition system.

Figure 21. One Agilent M9703A AXIe 12-bit digitizers and one M9536A embedded AXIe controller installed in the Agilent M9502A 2-slot AXIe chassis.

Ordering information

Model	Description
M9703A	AXIe 12-bit Digitizer with on-board processing Includes: -Software, example programs and product information on CD -Return to Agilent Warranty extended to 3 years

Configurable options		
Sampling rate		
✓	M9703A-SR1	1 GS/s sampling rate version (2 GS/s sampling rate with -INT option)
	M9703A-SR2	1.6 GS/s sampling rate version (3.2 GS/s sampling rate with -INT option)
Bandwidth		
✓	M9703A-F05	Input Frequency: DC to 650 MHz
	M9703A-F10	Input Frequency: DC to 2 GHz (not interleaved) Input Frequency: DC to 1 GHz (interleaved)
Front-end		
	M9703A-FRF	Optimized dynamic range
Memory		
✓	M9703A-M10	1 GB (64 MS/ch) acquisition memory
	M9703A-M40	4 GB (256 MS/ch) acquisition memory
	M9703A-M16	16 GB (1 GS/ch) acquisition memory
Firmware		
✓	M9703A-DGT	Digitizer firmware
	M9703A-DDC	Wideband real-time digital down-conversion
	M9703A-LDC	Limited-bandwidth real-time digital down-conversion 50 MHz real-time analysis bandwidth with -SR1 80 MHz real-time analysis bandwidth with -SR2
	M9703A-INT	Interleaved channel sampling functionality
	M9703A-FDK	FPGA programming access

✓ *These options represent the standard configuration of the M9703A.*

Typical system configuration

Model	Description
M9703A	AXIe digitizer, 12-bit, 8-channel
M9505A	5-slot AXIe chassis
M9047A	PCIe deskstop PC adapter: Gen2, x8

Advantage Services: Calibration and warranty	
Agilent Advantage Services is committed to your success throughout your equipment's lifetime.	
M9703A-UK6	Commercial calibration certificate calibration with test data
Included	3-year warranty (return to Agilent), standard
R-51B-001-5Z	5-year return to Agilent warranty assurance plan

The modular tangram

The four-sided geometric symbol that appears in this document is called a tangram. The goal of this seven-piece puzzle is to create identifiable shapes—from simple to complex. As with a tangram, the possibilities may seem infinite as you begin to create a new test system. With a set of clearly defined elements—hardware, software—Agilent can help you create the system you need, from simple to complex.

Challenge the Boundaries of Test

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Product specifications and descriptions in this document subject to change without notice.

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